bit:	63	48 47		32 31		16 15		0
vs:	vs[3]		vs[2]		vs[1]		vs[0]	
	+		+		+		+	
vt:	vt[3]		vt[2]		vt[1]		vt[0]	
	↓		↓		↓		↓	
vd:	vs[3]+vt[3]		vs[2]+vt[2]		vs[1]+vt[1]		vs[0]+vt[0]	

FIG. 1

(Prior Art)

COMPUTER SYSTEM 212

PROCESSOR 201

RF 204

Optional
DISPLAY
DEVICE 205

ROM 203
Non Volatile

Optional
ALPHANUMERIC
INPUT 206

RAM 202
Volatile

Optional
CURSOR
CONTROL 207

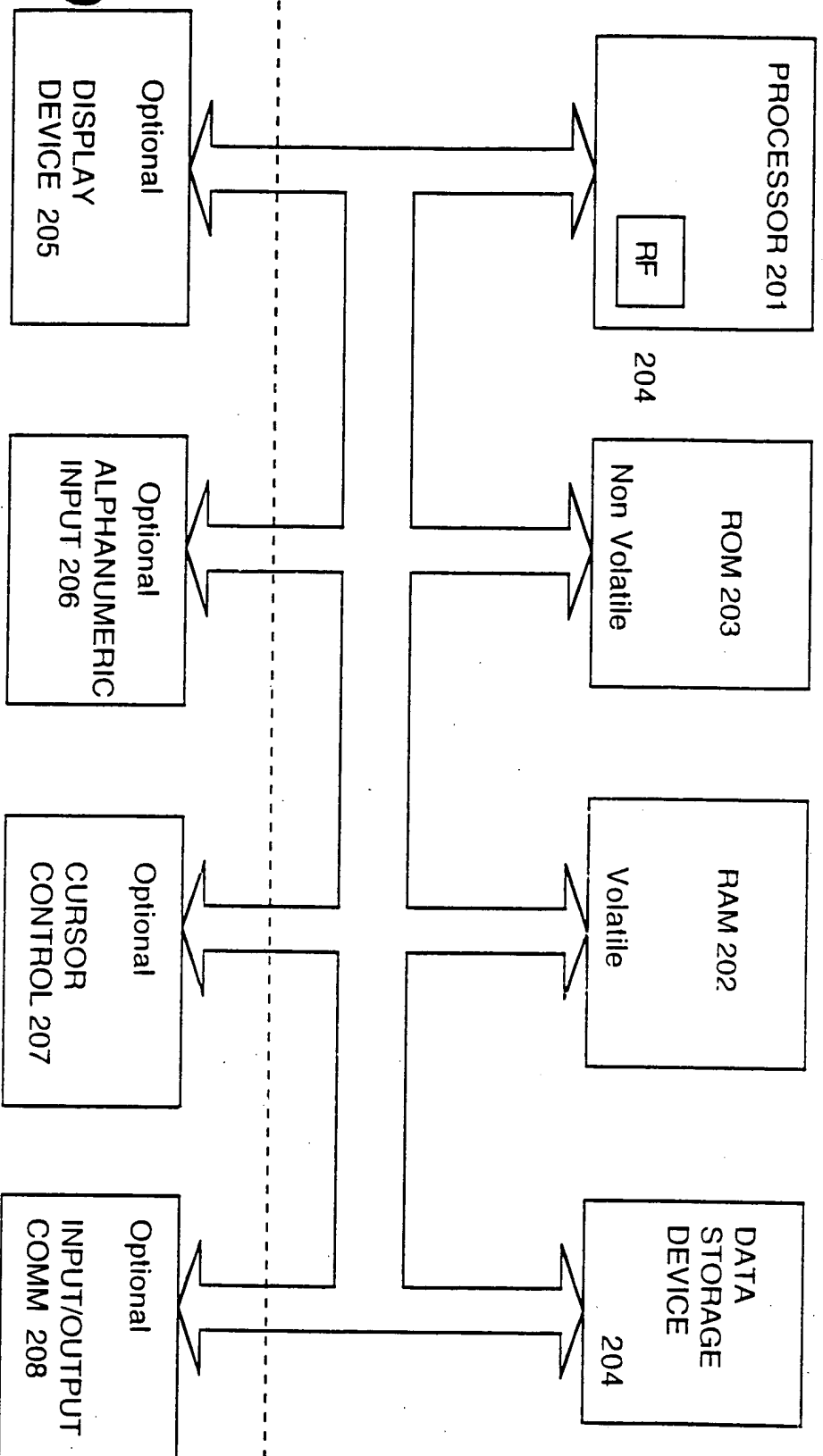DATA
STORAGE
DEVICE
204

Optional
INPUT/OUTPUT
COMM 208

FIG. 2

FIG. 3

300

To Main Memory

Vector Load/Store Unit 318

Register File 304

63   0
vs 306

63   0
vt 308

...

63   0
vd 310

320

314

322

SIMD Vector Unit
302

191   0
Accumulator 312

324

316

326

FIG. 4

ALU 402

adder/subtractor 404

ACC 312

vs

vt

Fetch arithmetic instruction — 502

Decode the arithmetic instruction — 504

Read operand registers — 506

Execute the arithemtic instruction on each element of the operands — 508

Write the resulting elements into accumulator — 510

Transform the resulting elements into N-bits — 512

Store the transformed elements into memory — 514

Done — 516
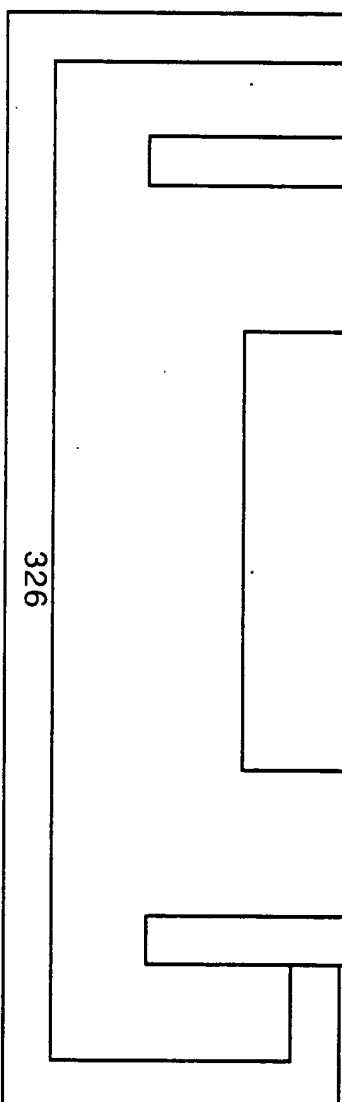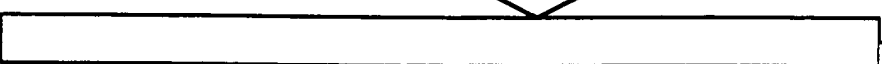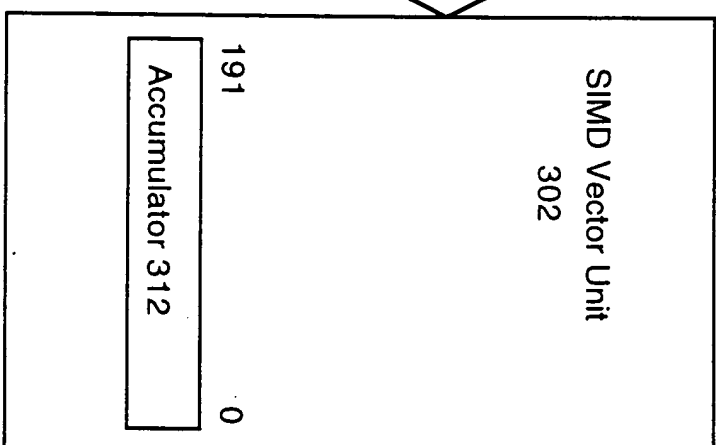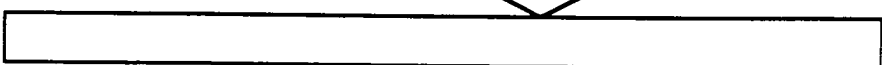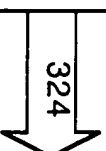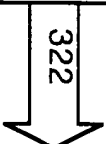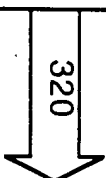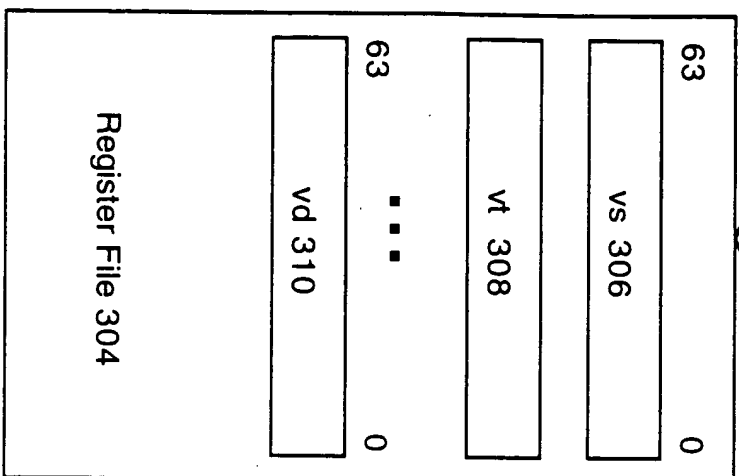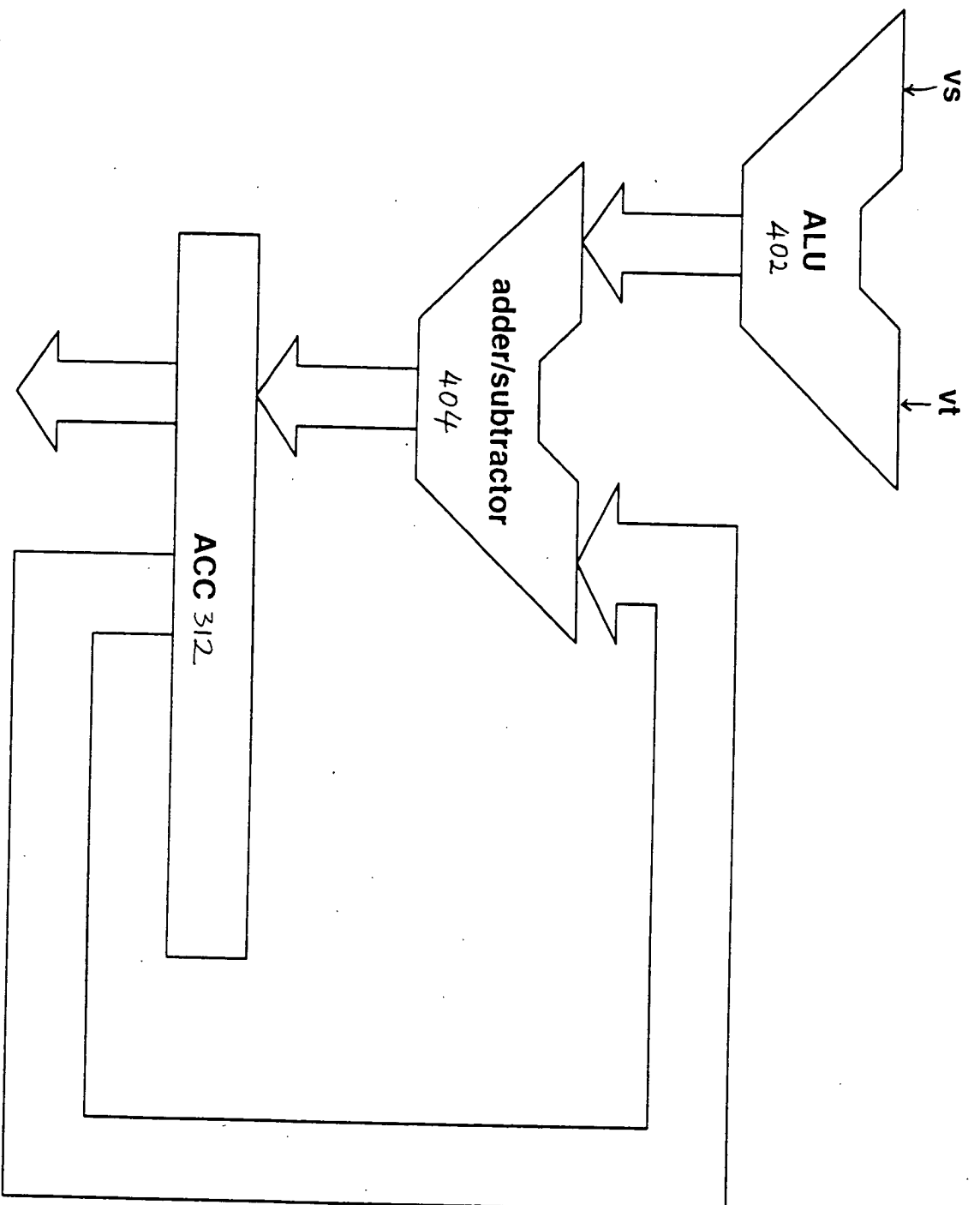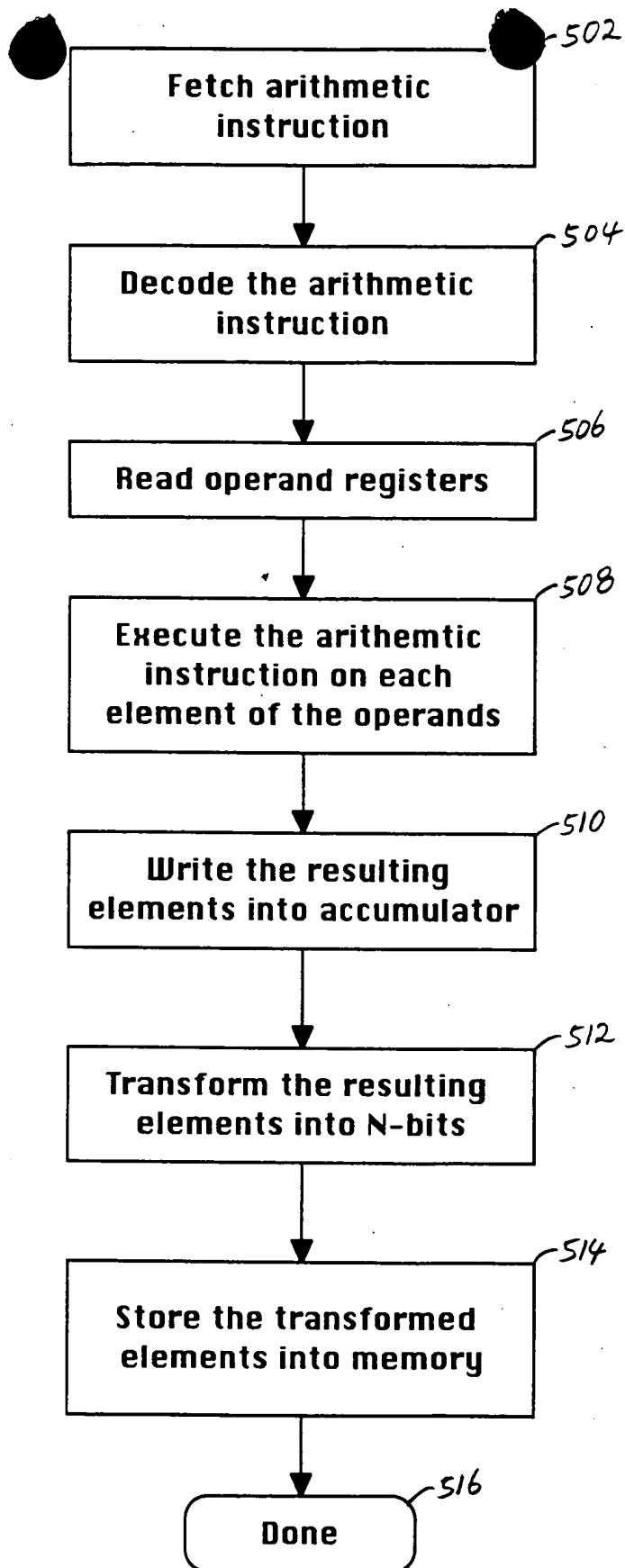
FIG. 5

QH DATA TYPE ELEMENT SELECT FORMAT

vt:

63	48 47	32 31	16 15	0	
D	C	B	A		~600
A	A	A	A		~602
B	B	B	B		~604
C	C	C	C		~606
D	D	D	D		~608
D	C	B	A		~610

FIG. 6

OB DATA TYPE ELEMENT SELECT FORMAT

vt:

63	56 55	48 47	40 39	32 31	24 23	16 15	8 7	0	
H	G	F	E	D	C	B	A	~700
A	A	A	A	A	A	A	A	~702
B	B	B	B	B	B	B	B	~704
C	C	C	C	C	C	C	C	~706
D	D	D	D	D	D	D	D	~708
E	E	E	E	E	E	E	E	~710
F	F	F	F	F	F	F	F	~712
G	G	G	G	G	G	G	G	~714
H	H	H	H	H	H	H	H	~716
H	G	F	E	D	C	B	A	~718

FIG. 7

FIG. 8

FIG. 9

191   C+F   144 143   B+E   96 95   A+D   48 47   1FFFD   0 ~904

63   C   48 47   B   32 31   A   16 15   FFFF   0 ~900

F   +   E   +   D   +   FFFF   +   ~902